IT IS CLAIMED:

1. In an array of non-volatile memory cells formed in rows and columns on a semiconductor substrate with elongated source and drain diffusions extending between columns of cells and word lines extending across rows of cells, wherein individual cells have a first channel segment between adjacent source and drain diffusions in the substrate that is controlled by at least one storage element and a second channel segment that is controlled by a select gate portion of one of the word lines, an improved structure comprising:

trenches formed in the semiconductor substrate as part of the cells, said second channel portion of the individual cells being provided along at least a sidewall of one of the trenches and the select gate being positioned in the trench,

elements of the source and drain diffusions and the first and second channel segments of adjacent cells being formed in a regular non-mirrored pattern in a direction across the array through these elements, and

elongated third gates extending across the array along and capacitively coupled with the storage elements.

2. The memory structure of claim 1, wherein the elongated third gates are erase gates that have lengths extending in a direction along rows of storage elements and which are individually positioned between adjacent rows of storage elements in a manner to have capacitive coupling with edges of the storage elements of at least one of said adjacent rows.

3. The memory structure of claim 1, wherein the elongated third gates are steering gates that have lengths extending across columns of storage elements and are individually positioned to have capacitive coupling with top surfaces of the storage elements of at least one column and underlie said word lines.

4. The memory structure of any one of claims 1-3, wherein one of the trenches is positioned between each of adjacent columns of storage elements, and the

source and drain diffusions are positioned at the bottom of the trenches and extend upwards along a sidewall of the trenches opposite to the second channel portion.

5. The memory structure of any one of claims 1-3, wherein one of the trenches passes through the individual cells and said second channel portion of the individual cells is provided along two sidewalls and a bottom surface of the channel, said source and drain diffusions being formed in a surface of the substrate outside of the trenches.

6. The memory structure of claim 5, wherein the individual cells include two storage elements positioned along a surface of the substrate on opposite sides of the trench.

7. The memory structure of claim 5, wherein the storage elements are conductive floating gates.

8. The memory structure of claim 5, wherein the storage elements are charge trapping dielectric layers.

9. The memory structure of any one of claims 1-3, wherein the storage elements are conductive floating gates.

10. The memory structure of any one of claims 1-3, wherein the storage elements are charge trapping dielectric layers.

11. An array of non-volatile memory cells on a semiconductor substrate, comprising:

elongated source and drain diffusions having their lengths extending in a first direction and being spaced apart in a second direction, the first and second directions being orthogonal to each other,

an array of floating gates arranged in columns extending in the first direction and rows extending in the second direction, individual memory cells having one edge of their floating gates positioned over one of the diffusions,

trenches in the substrate adjacent opposite edges of the floating gates in the second direction, said trenches containing another one of the diffusions,

elongated control gates having lengths extending in the second direction along rows of floating gates and being capacitively coupled with the sidewalls of the trenches that are positioned immediately adjacent the floating gates, and

elongated erase gates having lengths extending in the second direction across the array along and capacitively coupled with rows of floating gate edges.

12. The memory cell array of claim 11, wherein the source and drain diffusions are formed in the bottoms of the trenches and on a surface of the semiconductor substrate.

13. The memory cell array of claim 11, wherein the source and drain diffusions are formed in a bottom and one side of the trenches.

14. An array of non-volatile memory cells on a semiconductor substrate, comprising:

elongated source and drain diffusions having their lengths extending in a first direction and being spaced apart in a second direction, the first and second directions being orthogonal to each other,

an array of floating gates arranged in columns extending in the first direction and rows extending in the second direction, individual memory cells having one edge of their floating gates positioned over one of the diffusions,

trenches in the substrate adjacent opposite edges of the floating gates in the second direction, said trenches containing another one of the diffusions,

elongated word lines having lengths extending in the second direction over rows of floating gates and having select gates capacitively coupled with the sidewalls of the trenches that are positioned immediately adjacent the floating gates, and

elongated steering gates having lengths extending in the first direction across the array over and capacitively coupled with columns of floating gates.

15. The memory cell array of claim 14, wherein the source and drain diffusions are formed in the bottoms of the trenches and on a surface of the semiconductor substrate.

16. The memory cell array of claim 14, wherein the source and drain diffusions are formed in a bottom and one side of the trenches.

17. An array of non-volatile memory cells on a semiconductor substrate, comprising:

elongated trenches formed in the substrate with their lengths extending in a first direction and being spaced apart in a second direction, the first and second directions being orthogonal to each other,

elongated source and drain diffusions with their lengths extending in the first direction and being spaced apart in the second direction such that first alternate diffusions are formed in the substrate along a bottom of individual trenches and that second alternate diffusions are formed in the substrate along a top surface thereof,

an array of floating gates spaced apart across the top surface of the substrate in the first direction and individually spanning between a trench and substrate surface diffusion in the second direction without extending downward into a trench,

elongated word lines having lengths extending in the second direction over floating gates and being spaced apart in the first direction, said word lines having select gates extending downward into the trenches to capacitively couple with opposing sidewalls of the trenches, and

elongated third gates extending across the array and individually being capacitive coupled with a plurality of floating gates.

18. The memory cell array of claim 17, wherein the elongated third gates are erase gates having lengths extending in the second direction and which are

spaced apart in the first direction, said third gates having capacitive coupling with edges of adjacent floating gates.

19. The memory cell array of claim 17, wherein the elongated third gates are steering gates that have lengths extending in the first direction and which are spaced apart in the second direction, said third gates having capacitive coupling with top surfaces of floating gates over which they pass.

20. An array of non-volatile memory cells on a semiconductor substrate, comprising:

elongated trenches formed in the substrate with their lengths extending in a first direction and being spaced apart in a second direction, the first and second directions being orthogonal to each other,

elongated source and drain diffusions with their lengths extending in the first direction being formed in the substrate along a bottom and extending upward along one sidewall of the individual trenches to a top surface of the substrate but being absent from an opposite sidewall of the individual trenches, said one sidewall of the trenches facing the same direction,

an array of floating gates spaced apart across the top surface of the substrate in the first direction and spanning between the trenches in the second direction without extending downward into the trenches, and

elongated word lines having lengths extending in the second direction over floating gates and being spaced apart in the first direction, said word lines having select gates extending downward into the trenches to capacitively couple with said opposite trench sidewalls.

21. The memory cell array of claim 20, which additionally comprises elongated steering gates having lengths extending in the first direction and being spaced apart in the second direction, said steering gates extending under the word lines and over floating gates with capacitive coupling between the steering gates and the floating gates.

22. The memory cell array of claim 20, which additionally comprises elongated control gates having lengths extending in the second direction and being spaced apart in the first direction, said control gates being capacitively coupled with edges of floating gates along which the individual control gates are positioned.

23. A process of fabricating a non-volatile memory cell array, comprising:

forming strips of polysilicon across a semiconductor substrate with a layer of dielectric therebetween, the polysilicon strips being elongated in a first direction across the substrate and being spaced apart in a second direction, wherein the first and second directions are orthogonal with each other,

etching trenches into the substrate between at least every other one of the polysilicon strips, said trenches being defined by positions of the polysilicon strips and having lengths extending in the first direction,

thereafter implanting ions along the lengths of the trenches to form elongated sources and drains in said trenches,

thereafter separating the strips of polysilicon into individual floating gates, thereby forming a two-dimensional array of floating gates,

forming a first plurality of elongated gates extending across the array of floating gates in the first direction that extend into the trenches crossed by them, and

forming a second plurality of elongated gates.

24. The process of claim 23, wherein the trenches are etched into the substrate between every one of the polysilicon strips and ions are implanted into both the bottom and only one of opposing sidewalls of the individual trenches.

25. The process of either one of claims 23 or 24, wherein the second plurality of elongated gates are elongated in the first direction and positioned between the first plurality of elongated gates in the second direction.

26. The process of either one of claims 23 or 24, wherein the second plurality of elongated gates are elongated in the second direction and vertically positioned between the first plurality of elongated gates and the floating gates.

27. A process of fabricating a non-volatile memory cell array, comprising:

forming strips of polysilicon across a semiconductor substrate with a layer of dielectric therebetween, the polysilicon strips being elongated in a first direction across the substrate and being spaced apart in a second direction, wherein the first and second directions are orthogonal with each other,

etching trenches into the substrate in each space between the polysilicon strips, a width of said trenches in the second direction being defined by positions of the polysilicon strips and having lengths extending in the first direction,

thereafter implanting ions along the lengths of the trenches in their bottoms and only one of opposing sidewalls to form elongated sources and drains in said trenches,

thereafter separating the strips of polysilicon into individual floating gates, thereby forming a two-dimensional array of floating gates, and

forming a plurality of elongated gates extending across the array of floating gates in the first direction that extend into the trenches crossed by them.

28. The process of claim 27, wherein separation of the strips of polysilicon into individual floating gates includes doing so by reference to the positions of the first plurality of elongated gates.

29. An array of non-volatile memory cells that individually include at least one storage element transistor and at least one select transistor in series between source and drain regions of a substrate, comprising:

a recess in a surface of the substrate,

said at least one storage element of the individual cells being positioned on the surface of the substrate with a first dielectric therebetween and adjacent one edge of the recess,

a gate extending into the recess with a second dielectric therebetween in order to form a channel of the select transistor along opposing walls and a bottom surface of the recess, and

components of the source and drain diffusions, recesses and storage elements being formed in a regular non-mirrored pattern in a direction across the array through these components.

30. The array of claim 29, wherein the storage elements are conductive floating gates.

31. The array of claim 29, wherein the storage elements are charge trapping dielectric material.

32. An array of non-volatile memory cells, the memory cells individually comprising:

source and drain regions formed in a planar surface of a substrate a distance apart from each other, thereby defining a semi-conductive channel of the memory cell therebetween,

first and second memory storage elements positioned over the planar substrate surface adjacent the respective source and drain regions,

a recess formed in the substrate surface between the first and second storage elements in a manner to have sidewalls and a bottom, and

a select transistor gate extending into the recess in a manner to have field coupling with the recess sidewalls and bottom through a dielectric layer therebetween, thereby utilizing the recess sidewalls as part of the memory cell channel.

33. The array of claim 32, wherein the recess is from 500 to 2000 Angstroms in depth below the substrate surface.

34. The array of claim 32, wherein the storage elements are conductive floating gates.

35. The array of claim 32, wherein the storage elements are charge trapping dielectric material.